PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

DONALDSON & BURKINSHAW
P.O. Box 3667
Singapore 905667
SINGAPOUR

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10 FEB 2000

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT
(PCT Rule 71.1)

Date of mailing *(day/month/year)*	03.02.2000
Applicant's or agent's file reference SGS/49424	IMPORTANT NOTIFICATION

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/SG97/00055	31/10/1997	31/10/1997

Applicant
SGS-THOMSON MICROELECTRONICS ASIA ..... et al.

DEADLINE

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/	Authorized officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Finnie, A Tel. +49 89 2399-3251

Form PCT/IPEA/416 (July 1992)

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26C1

PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
SGS/49424		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/SG97/00055	31/10/1997	~~31/10/1997~~
International Patent Classification (IPC) or national classification and IPC H04J3/06		
Applicant SGS-THOMSON MICROELECTRONICS ASIA ..... et al.		

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FEB -9 2001
TC 2600 MAILROOM

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
27/05/1999	03.02.2000
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Frey, R Telephone No. +49 89 2399 7522

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/SG97/00055

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-8,10-14	as originally filed			
9,15	as received on	21/10/1999	with letter of	15/10/1999

Claims, No.:

1-13(part), 18(part)-25	as originally filed			
13(part) - 18(part)	as received on	21/10/1999	with letter of	15/10/1999

Drawings, sheets:

1/5-5/5	as originally filed

2. The amendments have resulted in the cancellation of:

☐ the description, pages:
☒ the claims, Nos.: 26-29
☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-25
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-25
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-25
	No:	Claims	

2. Citations and explanations

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V

Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Claim 1 relates to an apparatus for depacketising and aligning packetised input data having an input memory, a depacketiser and data processing means.
According to the present invention the function of the depacketiser and the data processor are combined on the same processor while simpler tasks are performed by a dedicated payload counter and word formatter.
Such an apparatus for depacketising and aligning packetised input data is neither taught, nor rendered obvious, alone or in combination, by the prior art documents cited in the International Search Report, which generally deal with apparatus for depacketising and aligning input data without any hint to the claimed specific allocation of functions to the data processor, payload counter and word formatter.
Claim 1 is therefore novel and considered to involve the required inventive step, Articles 33(2) and (3) PCT. The subject-matter of claim 1 is also industrially applicable.

The same applies to independent claim 24 which generalises the input memory as being a means for transferring the data words to the data processing means and independent claims 13 and 25 defining a method for depacketising and aligning packetised input data corresponding to independent claims 1 and 24, respectively. Claims 13, 24 and 25 therefore, equally meet all the requirements of Article 33 PCT.

Dependent claims 2 to 12 and 14 to 23 relate to particular embodiments of the apparatus and the method defined by the independent claims to which they refer and are thus equally novel, inventive and industrially applicable.

Re Item VII
Certain defects in the international application

1. The following drafting errors are present in the claims.

1.1 On page 17, line 18 (claim 6) the wording "to the data" is superflux.

1.2 On page 19, lines 11 to 12 (claim 15) it should read " and to *generate said* payload size signal".

2. The claims do not include reference signs in parentheses where features shown in the drawings are referred to, Rule 6.2.(b) PCT.

3. In claim 5 the wording "as appended directly or indirectly to claim 2" is unclear (Article 6 PCT).

4. The general "spirit and scope" statement in the last paragraph of the description is unclear, and when used to interpret the claims renders them also unclear, contrary to Article 6 PCT.

Re Item VIII
Certain observations on the international application

Although claims 6, 11 and 12 are directed to an apparatus, they contain features relating to activities in which the use of a physical entity is implied (e.g. doing something by means of), namely "is controlled", "is removed ... and relaced" in claim 6; and "extracts" in claims 11 and 12.

Those features are regarded as features of a method. Therefore, these claims contain a mixture of apparatus and method features introducing doubt as to the category of the claims (Article 6 PCT).

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal whereby to cause payload units which form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing these in said input buffer;

transferring said data words to the data processing means.

In a particular form of the invention, a single programmable processor core is used as the Data Processor of the system for processing of the de-packetized data; the detection of sync-word, decoding of the packet ID, payload size, timing and necessary side information of the data packet which take up only little processing cycles are instead performed by the same Data Processor in software to provide the necessary flexibility. The De-Packetizer hardware can be simplified to an implementation with only the Payload Counter which controls size of payload transferred and the Word Formatter to align the payload data to the Data Processor word format.

The writing of de-packetized data to the Input Buffer 404 and the reading of it by the Digital Signal Processor 405 can be organized in a circular buffer mode to increase efficiency. In another embodiment of the current invention, it is advantageous to combine the Input Buffer 404 with any Data/Program Memory 411. The present invention does not exclude embodiments with multiple word formatter and input buffers, as it can be easily expanded to handle de-interleaving, de-packetization and alignment of multiple packetized input data.

With the coupling of the payload counter and word formatter with data input interface and input FIFO, the present invention provides a very low cost but efficient implementation for de-packetizing and aligning packetized input data. The payload counter and word formatter combination releases data processing load from the data processor for the system. Its capability of aligning the de-packetized data for the input buffer allows saving of memory size needed for the input buffer and hence saving of implementation cost. The described arrangements of the invention have the ability of sharing the data processing task and the part of the de-packetizing task with the same data processor and therefore provides all needed flexibility in the de-packetizing task.

The described arrangements have been advanced merely by way of explanation and many modifications may be made thereto without departing from the spirit and scope of the invention which includes every novel feature and combination of novel features herein disclosed.

effecting data processing on the data packet represented by the data words transferred thereto, using the transferred data words.

14. A method as claimed in claim 13 wherein the input data is transferred to the input memory via an data input interface which performs hand shaking with a packetized data source of said input data.

15. A method as claimed in claim 13 or claim 14 including the step of generating a level filled signal when the input data received by the input memory is such as to fill the input memory to a predetermined level, and causing said data processing means to effect said detecting, identifying and determining payload size of the data packet, and to said generate payload size signal, pursuant to generation of the level filled signal.

16.(Amended) A method as claimed in claim 15 including the step of generating an interrupt signal from said level filled signal and directing said interrupt signal to said data processing means to cause said data processing means to effect said receiving and outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and to generate said payload size signal.

17. A method as claimed in claim 15 or claim 16, as appended directly or indirectly to claim 14, including the step of generating and directing to said data input interface a further level filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, and causing said data input interface to generate, responsive to receipt thereby of said further level filled signal, a data request signal for direction to said packetized data source, indicative of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source.

18. A method as claimed in any one of claims 13 to 17 wherein the input memory is controlled whereby said input data comprising a said packet is removed from the input memory and replaced by fresh input data pursuant to the transfer of said words representing that data packet to the data processor, and wherein a step comprising said receiving and outputted input

size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal whereby to cause the payload units to be outputted from the input memory to the word formatter; and

means for transferring the data words to the data processing means, to effect said separate receiving of said payload.

25. A method for depacketizing and aligning packetized input data comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying and determining the size of a payload of a data packet of the input outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal whereby to cause payload units which form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing the in said input buffer;

transferring said data words to the data processing means.

26. (Deleted)

27. (Deleted)

28. (Deleted)

29. (Deleted)

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

United States Patent and Trademark Office
(Box PCT)
Crystal Plaza 2
Washington, DC 20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 22 June 1999 (22.06.99)	
International application No. PCT/SG97/00055	**Applicant's or agent's file reference** SGS/49424
International filing date (day/month/year) 31 October 1997 (31.10.97)	**Priority date** (day/month/year)
Applicant HUI, Yau, Wei, Lucas et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

27 May 1999 (27.05.99)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer C. Carrié

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
SGS/49424		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/SG 97/ 00055	31/10/1997	
Applicant		
SGS-THOMSON MICROELECTRONICS ASIA ..... et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. [ ] **Certain claims were found unsearchable** (see Box I).

2. [ ] **Unity of invention is lacking** (see Box II).

3. [ ] The international application contains disclosure of a **nucleotide and/or amino acid sequence listing** and the international search was carried out on the basis of the sequence listing
   - [ ] filed with the international application.
   - [ ] furnished by the applicant separately from the international application,
     - [ ] but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in the international application as filed.
   - [ ] Transcribed by this Authority

4. With regard to the **title,**
   - [X] the text is approved as submitted by the applicant
   - [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   - [X] the text is approved as submitted by the applicant
   - [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this International Search Report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is:
   Figure No. 3
   - [ ] as suggested by the applicant.
   - [X] because the applicant failed to suggest a figure.
   - [ ] because this figure better characterizes the invention.
   - [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/ 97/00055

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04J3/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DOBINSON R W ET AL: "INTERFACING TO ETHERNET USING VLSI PROTOCOL CHIPS" INTERFACES IN COMPUTING, vol. 3, no. 3/04, September 1985, pages 173-187, XP002005672 see page 174, line 10 - line 24 see page 178, line 5 - line 41 see page 179, line 6 - line 139 ---	26,28
A	DE 42 17 911 A (BUNDESREP DEUTSCHLAND) 2 December 1993 see column 1, line 64 - column 2, line 62 ---	1,13,24, 25
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 July 1998	24/07/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Van den Berg, J.G.J.

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT 97/00055

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 798 932 A (MATSUSHITA ELECTRIC IND CO LTD) 1 October 1997 see page 5, line 20 - line 25 see page 6, line 35 - line 41 see page 7, line 21 - line 27 see page 8, line 22 - line 46 see page 11, line 55 - page 12, line 8	1,13,24, 25
A	US 5 534 937 A (ZHU QIN-FAN ET AL) 9 July 1996 see column 3, line 3 - line 13 see column 3, line 59 - column 4, line 16 see column 4, line 58 - line 62	1,13,24, 25
A	EP 0 648 034 A (BELL TELEPHONE MFG ;ALCATEL NV (NL)) 12 April 1995 see column 2, line 32 - line 45 see column 3, line 54 - column 4, line 18 see column 8, line 33 - line 42 see column 9, line 12 - line 24	2

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 97/00055

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 4217911 A	02-12-1993	NONE	
EP 0798932 A	01-10-1997	JP 10093960 A	10-04-1998
US 5534937 A	09-07-1996	EP 0704134 A	03-04-1996
		JP 8511932 T	10-12-1996
		WO 9528802 A	26-10-1995
EP 0648034 A	12-04-1995	US 5453980 A	26-09-1995

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WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H04J 3/06

A1

(11) International Publication Number: WO 99/23776

(43) International Publication Date: 14 May 1999 (14.05.99)

(21) International Application Number: PCT/SG97/00055

(22) International Filing Date: 31 October 1997 (31.10.97)

(71) Applicants *(for all designated States except US)*: SGS-THOMSON MICROELECTRONICS ASIA PACIFIC (PTE) LTD. [SG/SG]; 28 Ang Mo Kio Industrial Park 2, Singapore 569508 (SG). SGS-THOMSON MICROELECTRONICS S.A. [FR/FR]; 7, avenue Galliéni, F-94253 Gentilly Cedex (FR).

(72) Inventors; and

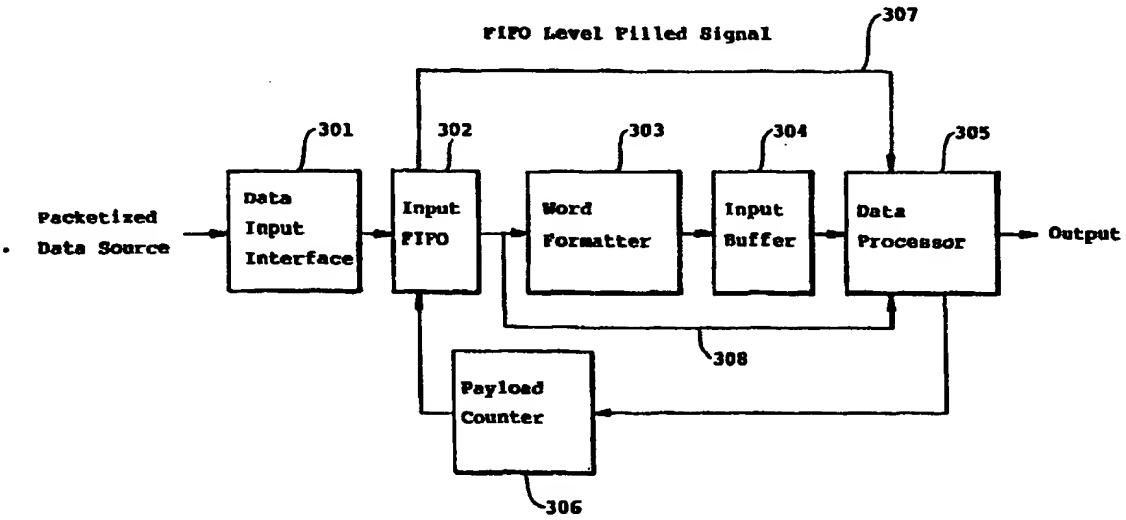
(75) Inventors/Applicants *(for US only)*: HUI, Yau, Wei, Lucas [SG/SG]; 10H Braddell Hill #24-31, Singapore 579727 (SG). LABORIE, Jean, Louis [FR/FR]; 6, rue du Fournet, F-38120 Saint Egrève (FR). LASSURE, Gaël [FR/SG]; 20, rue des Bois, F-77166 Grisy Suisnes (FR).

(74) Agent: DONALDSON & BURKINSHAW; P.O. Box 3667, Singapore 905667 (SG).

(81) Designated States: JP, SG, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: APPARATUS AND METHOD FOR DEPACKETIZING AND ALIGNING PACKETIZED INPUT DATA



(57) Abstract

Apparatus for depacketizing and aligning packetized input data. Data processing means (305) receives the input data via an input memory (301) and detects, identifies and determines payload size of a data packet of the input data. The data processing means (305) generates a payload size signal indicative of the size of the payload. A word formatter (303) receives units of the payload from the input memory (301) and gathers and aligns these to form data words. A payload counter (306) controls flow of input data from the input memory (301) to the word formatter (303) in accordance with the payload size signal. An input buffer (304) receives the data words from the word formatter (303), stores these and transfers them to the data processing means (305) for effecting data processing.

FOR THE PURPOSES OF INFORMATION ONLY

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APPARATUS AND METHOD FOR DE-PACKETIZING AND ALIGNING PACKETIZED INPUT DATA

DETAILED DESCRIPTION OF THE INVENTION

(1) Field of the Invention

This invention relates to apparatus and method for de-packetizing and aligning packetized input data.

(ii) Prior Art

In data retrieval or communication systems, digital data or digitized multimedia information which can be, potentially, large or variable in size is normally packetized before storage or transmission. This process breaks the data into smaller packets where each packet contains one or more detectable synchronization patterns called sync-word, necessary information about the packet, and a payload of a smaller partition of the original data. The information about the packet may consist of a packet identification (ID), size of the payload contained in the current packet, timing information, and any necessary side information.

In applications where there could be multiple sources of data, for example shared data network or multimedia audio/visual information for local data storage device, each source of data is packetized and the resulting packets from all sources are interleaved before transmission or storage. The packet ID is used to identify the data source of each packet. Timing information, which may be in the form of time stamps or temporal references, is used for ordering of the packets or for synchronization between each data source for transmission or presentation.

Information related to both multimedia audio and video data is often very large in size, and therefore data compression techniques such as MPEG video and audio compression techniques

are usually applied before packetization. Packetization in this case may also follow the method as specified by the MPEG Systems specifications.

With respect to data retrieving operations, packets received from a communication system or read from local storage are required to be de-packetized before processing by each respective data processor. The de-packetization process includes, first, detection of the sync-word, follow by verification of the packet ID, extraction of timing and necessary side information, determining the payload size and, finally, extraction and concatenation of the payload to reconstruct the data. The de-packetized data may be passed to a data processor for further processing. For example, the data processor for MPEG compressed audio data will be a corresponding MPEG audio decoder; furthermore, this audio decoder may be implemented using programmable DSP (Digital Signal Processor).

Figure 1 illustrates a block diagram of a prior art system. Packetized data is received via a data input interface 101, where hand shaking with the packetized data source is performed, and also, if necessary, serial-to-parallel conversion is effected. The received packetized data is processed by a De-packetizer 103. In order to handle possible jitters in overall transmission rate of the packetized data source and the processing speed of the de-packetizer, an Input FIFO (first-in-first-out memory) 102 is inserted in between the data input interface 101 and the de-packetizer 103. The de-packetizer 103 can be a dedicated and fixed function hardware or a programmable processor performing the de-packetization process, as described, to produce the de-packetized data. The de-packetized data is placed into an Input Buffer 104 before being read by Data Processor 105.

The size of the Input Buffer 104 is determined by the nature and type of the data involved, the processing bandwidth of the data processor 105 and, possibly, synchronization requirements of other processes outside the system. For example, it may serve as a delay buffer for synchronization of an audio data stream to an external video data stream, or a temporal storage buffer such that it can feed regularly to a high speed data processor a block of data, at a rate higher that the input rate.

In Figure 2, a block diagram of another prior art system prior art is illustrated. In order to reduce overall system cost and improve performance of the data processor, single port system RAM (random access memory) coupling to the system bus of the data processor 205 serves as the Input Buffer 204, and a DMA Controller (direct memory access controller) 206 is normally used for transferring the de-packetized data from the de-packetizer 203 to the input buffer 204 via the system bus. The Input Buffer 204 may be optimized in size by using a circular buffer technique.

It is likely that the system RAM and the input data (packetized or de-packetized) do not share the same word format in terms of number of bit resolution. For example, the MPEG systems data is byte aligned and most DSP systems (system bus, system RAM, etc.) use sixteen or more bits per word for performance reasons. It is a task for the de-packetizer 203 to align the de-packetized data to the word format required by the data processor before outputting it to the Input Buffer 204, since this input buffer belongs also to part of the data processor system RAM.

In most systems implementations, flexibility in the De-Packetizer is required, for handling variations in the decoding of the sync-word, ID, timing and necessary side information in each packet; hence, a programmable processor core is very suitable for these jobs. On the other hand, the De-Packetizer is also required to perform simple but highly repetitive tasks of reading payload from the data input interface, aligning the de-packetized data to the data processor word format, and moving the de-packetized and aligned data to the input buffer. A programmable processor core, is highly inefficient for such simple but highly repetitive tasks as it takes up a high percentage of the processing cycles.

A large FIFO may also be required as buffer memory in between the Data Input Interface and the De-Packetizer, due to the requirements of flexibility in the de-packetization process and inefficiencies of a programmable processor core for simple and highly repetitive tasks. Furthermore, additional memory must be associated with the programmable processor core for storing and processing of the necessary side information of the packets.

SUMMARY OF THE INVENTION

It is an object of the current invention to provide an improved apparatus and method for de-packetizating and aligning packetized input data.

In one aspect, the invention provides apparatus for depacketizing and aligning packetized input data, having:

an input memory for receiving storing, and output of the input data, and for outputting of units of a payload of a data packet of the input data;

data processing means for receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating a payload size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal whereby to cause the payload units to be outputted from the input memory to the word formatter; and

an input buffer for receiving said data words from the word formatter and storing these, and for transferring the data words to the data processing means, to effect said separate receiving of said payload;

said data processing means for effecting said data processing using the received said data words.

The apparatus may have a data input interface through which the input data is transferred to the input memory, said data input interface for performing hand shaking with a packetized data source of said input data.

The input memory may have a fullness level detector for generating a level filled signal when the input data received thereby is such as to fill the input memory to a predetermined level, and said data processing means may be responsive to generation of said level filled signal to execute said

receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating said payload size signal.

An interrupt controller may be provided for receiving said level filled signal and generating an interrupt signal pursuant to receipt thereof, said data processing means being arranged for receipt of said interrupt signal and, on receipt thereof, for executing said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal.

The input memory may have a further fullness level detector for generating and directing to said data input interface a further level filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, said data input interface being responsive to receipt of said further level filled signal to generate a data request signal for direction to said packetized data source, indicative of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source.

The input memory may be controlled whereby said input data comprising said packet is removed from the input memory and relaced by fresh input data , pursuant to the transfer to the data processing means of said words representing the data packet to the data the apparatus being arranged for repetitive depacketizing and aligning of data packets and data processing thereof, the data processing means being arranged for repetitively and alternatingly executing a step comprising said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal, and a step comprising said separately receiving and effecting data processing of the payload of the data packet.

The data processing means may include a digital signal processor, data/program memory, DMA controller and input buffer, each in data communication via a bus.

The word formatter may be arranged for generating a DMA request signal when a said data word is formed thereby, and the DMA controller is responsive to said DMA request signal to generate

and direct a transfer signal to the digital signal processor, the digital signal processor being responsive to the transfer signal to enable the DMA controller to move the data word from the word formatter to the input buffer for subsequent processing.

The input memory may comprise a first in first out memory.

The data processing means may be arranged to execute said detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID.

The data processing means may, pursuant to said detecting and identifying the data packet, extract timing information from the input data.

The data processing means may, pursuant to said detecting and identifying the data packet, extract side information from the input data.

The invention also provides a method for depacketizing and aligning packetized input data comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying and determining the size of a payload of a data packet of the input data outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal whereby to cause payload units which form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing these in said input buffer;

transferring said data words to the data processing means; and

effecting data processing on the data packet represented by the data words transferred thereto, using the transferred data words.

The input data may be transferred to the input memory via an data input interface which performs hand shaking with a packetized data source of said input data.

The method may include the step of generating a level filled signal when the input data received by the input memory is such as to fill the input memory to a predetermined level, and causing said data processing means to effect said detecting, identifying and determining payload size of the data packet, and to said generate payload size signal, pursuant to generation of the level filled signal.

The method may include the step of generating an interrupt signal from said level filled signal and directing said interrupt signal to said data processing means to cause said data processing means to effect said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and to generate said payload size signal.

The method may include the step of generating and directing to said data input interface a further level filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, and causing said data input interface to generate, responsive to receipt thereby of said further level filled signal, a data request signal for direction to said packetized data source, indicative of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source,

The input memory may be controlled whereby said input data comprising a said packet is removed from the input memory and relaced by fresh input data pursuant to the transfer of said words representing that data packet to the data processor. A step comprising said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal indicative of the size of the payload, and a step comprising effecting data processing of the payload may be repetitively and alternatingly executed.

A DMA request signal may be generated when a said word is formed, and applying the DMA request signal to a digital signal processor forming part of said data processing means to cause the digital signal processor to enable a DMA controller to move that data word from the word formatter to an input buffer of the data processor for subsequent processing.

The data processing means may execute said detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID.

The invention also provides apparatus for depacketizing and aligning packetized input data, having:

an input memory for receiving storing, and output of the input data, and for outputting of units of a payload of a data packet of the input data;

data processing means for receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating a payload size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal whereby to cause the payload units to be outputted from the input memory to the word formatter; and

means for transferring the data words to the data processing means, to effect said separate receiving of the data packet, when the stored data words complete said payload.

The invention also provides a method for depacketizing and aligning packetized input data comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying and determining the size of a payload of a data packet of the input data outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal whereby to cause payload units which form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing these in said input buffer;

transferring said data words to the data processing means.

The invention further provides apparatus for depacketising and aligning packetised input data, including data processing means which in use detects a payload of a data packet in the input data and processes the payload. The data processing means may repetitively and alternatingly execute functions of detecting payloads and processing these.

The invention further provides a method for depacketizing and aligning packetized input data wherein functions of detecting a payload of a data packet in the input data and processing the payload are effected separately by the same data processing means. The functions of detecting and processing may be repetitively and alternatingly executed sequentially with respect to successive data packets in the input data.

In a particular form of the invention, a single programmable processor core is used as the Data Processor of the system for processing of the de-packetized data; the detection of sync-word, decoding of the packet ID, payload size, timing and necessary side information of the data packet which take up only little processing cycles are instead performed by the same Data Processor in software to provide the necessary flexibility. The De-Packetizer hardware can be simplified to an implementation with only the Payload Counter which controls size of payload transferred and the Word Formatter to align the payload data to the Data Processor word format.

By combining the functions of the De-Packetizer which may require flexibility and the data processor implementation on the same programmable processor core, overall system complexity and cost can be minimized; furthermore, the use of a programmable processor core provides maximum flexibility to the De-Packetizer functions. On the other hand, the Payload counter and Word Formatter can take care of simple but repetitive tasks in such a way that overall system performance may be significantly enhanced with minimal implementation cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a prior art system for de-packetizing and processing data;

Figure 2 is a block diagram of a convention circuit for de-packetizing and processing data;

Figure 3 is a block diagram of an embodiment of a device for practising the present invention;

Figure 4 is a block diagram of an alternate embodiment of the present invention; and

Figure 5 is a flow charge illustrating an embodiment of part of the de-packetizing process according to the present invention.

DETAILED DESCRIPTION

Referring to Figure 3, Packetized data is input via the data input interface 301 to an input memory formed as an Input FIFO 302. When the Input FIFO 302 is filled to a predetermined level, data processing means in the form of a Data Processor 305 is signalled by FIFO Level Filled Signal 307, and packetized data is read from the Input FIFO 302 by the Data Processor 305 via path 308.

The Data Processor 305 scans the read packetized data for sync-word detection, ID checking,

payload size, timing and necessary side information decoding. When a valid packet is detected (by checking the sync-word and ID) and its payload size, timing and necessary side information decoded, the Data Processor stops reading packetized data directly from the Input FIFO 302, sets the Payload Counter 306 with the decoded payload size value, and returns to its normal data processing functions.

When the Payload Counter value is set, it starts loading the Word Formatter 303 with the payload. The Payload Counter counts as each unit of the payload is being transferred from the input FIFO 302 to the Word Formatter 303. The Word Formatter 303 gathers and aligns the received payload units according to the data processor word format. After a complete data word is formed in the Word Formatter 303, the data word is transferred to the Input Buffer 304. The Payload Counter 306 stops outputting of the payload from the Input FIFO 302 to the Word Formatter 303 after it has transferred the full payload size for the current packet. The Input FIFO 302 is then filled with the input packetized data, and the whole process is repeated again.

When the Input Buffer 304 is filled with certain required level of de-packetized data, the Data Processor 305 reads the de-packetized data from the Input Buffer 305 for further processing. The Data Processor 305 outputs the results of the processing.

Figure 4 illustrates in more detail an embodiment of a device for de-packetizing and aligning input data according to the present invention. A packetized data source (not shown) is connected to a Data Input Interface 401 which provides necessary signalling for the external packetized data source as well as possible format conversion. For example, the data input interface may be an embodiment of a serial-to-parallel adaptive which converts serial format data such as the I2S format to parallel data. The Data Input Interface 401 is coupled to an Input FIFO 402.

The Input FIFO 402 is a first-in-first-out memory buffer for accumulating input packetized data. A suitable size for the Input FIFO 402 depends on the requirements on process latency

and processing bandwidth of the Digital Signal Processor 405. Preferably the Input FIFO 402 has a storage format which is commonly usable by all input packetized data types. For example, the byte format is preferred as most packetized data and payload sizes are specified in unit byte size; in this case, the Data Input Interface 401 provides the necessary conversion of the input packetized data to byte format before storing it into the Input FIFO.

The Input FIFO 402 should contain at least one fullness level detector. This fullness level detector will generate a FIFO Level Filled Signal 407 when the Input FIFO is filled to a level which is equal to and optionally greater than a threshold level defined by the fullness level detector. This threshold level may be pre-defined or programmable. A second fullness level detector may be provided in the Input FIFO 402 for detecting if the Input FIFO is reaching a fullness level which cannot be filled further. This optional second fullness level detector will generate the necessary FIFO Full signal 412 to the Data Input Interface 401 which will in turn adjust a possible Data Request signal 413 to the external packetized data source for stop or start of transmission. Again, the level for fullness detection in the second fullness level detector can be pre-defined or programmable.

It is likely that for most applications the original data such as audio, video, and/or digital multimedia data is packetized and interleaved to form a data stream containing many packets. Before decoding and processing the data stream, it is de-interleaved if necessary and de-packetized. The de-packetization process starts by detecting the sync-word in each packet. This is initiated when the FIFO Level Filled Signal 407 is generated by the Input FIFO 402. The FIFO Level Filled Signal 407 is connected to an Interrupt Controller 410 which generate an Interrupt Signal 416 to the Digital Signal Processor 405. The Interrupt Controller 410 is used for arbitrating and prioritizing other possible signals in the device. In simplified systems, the Interrupt Controller may be removed, and the FIFO Level Filled Signal connected directly to Digital Signal Processor 405.

When the Digital Signal Processor 405 is signalled by the Interrupt Signal 416 generated by the FIFO Level Filled Signal 407, it switches to de-packetization process. In this process,

the Digital Signal Processor 405 reads directly from the Input FIFO 402 through path 414 and the system bus 408.

An embodiment of the de-packetization process is illustrated in Figure 5. Basically, on detection of the FIFO level filled signal 500, input packetized data is read, at step 501 and scanned at step 502 for the sync-word. The sync-word is defined based on applications or packet types, and is normally a digital pattern not easily found within the payload. After detection of the sync-word, the process checks at step 503 for the correct packet ID which may be used to differentiate packets from different data sources, types, or versions. Fault detection of the sync-word (emulation of the sync-word within payload data) is also minimized with the packet ID check. If there is wrong ID found, the process is reset to sync-word detection again. After checking the ID, the process executes step 504 at which the correct amount of packetized data is extracted from the Input FIFO for payload size, timing information, and necessary side information. Before exiting the de-packetization process (step 506), the Payload Counter (406) is set, at step 505 with payload size which defines the size of the data payload with the current packet.

The Input FIFO 402 may become empty while reading by the Digital Signal Processor 405 in the middle of the de-packetization process. In this case, the Digital Signal Processor exits the de-packetization process and return to its original process. When the FIFO is filled to the threshold level again, the Digital Signal Processor is signalled again and the de-packetization process resumes.

The Payload Counter 406 may include a decrement byte counter which can be set by the Digital Signal Process 405 through the System Bus 408, and some necessary control circuits. When the decrement byte counter is set with the payload size in terms of number of bytes (value greater than zero), a Payload request signal is sent to the Input FIFO 402 through path 415. If the Input FIFO 402 is not empty, the Word Formatter 403 is not full, and the decrement byte counter's value is greater than zero (payload request signal set), one byte will be transferred from the Input FIFO 402 to the Word Formatter 403, and the decrement byte

counter's value is reduced by one indicated by payload acknowledge signal from Input FIFO 402 through path 415. Hence, the Payload Counter 406 provides the function of moving the exact amount of payload data of each packet from the Input FIFO 402 to the Word Formatter 403.

The Word Formatter 403 aligns the payload data according to the word format of the Digital Signal Processor 405 and moves the aligned payload data to an Input Buffer 404. The word format is defined by bit width for a data word handled by the Digital Signal Processor 405. The Input Buffer 404, possible data/program memory 411 for the Digital Signal Processor, and the coupling System Bus 408 are supporting the same word format. For example, if the word format is given at 16-bit, two bytes must be received from the Input FIFO which is byte format memory to form a data word. When a data word is formed, it is transferred to the Input Buffer 404 via the System Bus 408. A DMA Controller 409 may be used to minimize the interruption to the Digital Signal Processor 405 for the transfer. In this case, when a data word is formed in the Word Formatter 403, a DMA request signal is generated to the DMA controller 409 which in turn make a Transfer request signal to the Digital Signal Processor. The Digital Signal Processor acknowledges the request when it releases the System Bus 408. The DMA Controller 409 will then move the data word from the Word Formatter to the Input Buffer through the system bus.

There may be packets with payload which contain a non-integer number of data words; for example, a packet with payload size in an odd number of bytes where the data word format is 16-bit. In this example, the last byte of the packet payload is stored in the word formatter until the first byte of the next packet payload is transferred to the word formatter. Therefore, the Word Formatter 403 provides all necessary data word alignment functions for the packet payload to the Input Buffer 404 to form the final de-packetized data which will be processed by the Digital Signal Processor 405. The Digital Signal Processor 405 may be replaced by any other suitable programmable processor core in other embodiments according to the present invention.

The writing of de-packetized data to the Input Buffer 404 and the reading of it by the Digital Signal Processor 405 can be organized in a circular buffer mode to increase efficiency. In another embodiment of the current invention, it is advantageous to combine the Input Buffer 404 with any Data/Program Memory 411. The present invention does not exclude embodiments with multiple word formatter and input buffers, as it can be easily expanded to handle de-interleaving, de-packetization and alignment of multiple packetized input data.

With the coupling of the payload counter and word formatter with data input interface and input FIFO, the present invention provides a very low cost but efficient implementation for de-packetizing and aligning packetized input data. The payload counter and word formatter combination releases data processing load from the data processor for the system. Its capability of aligning the de-packetized data for the input buffer allows saving of memory size needed for the input buffer and hence saving of implementation cost. The described arrangements of the invention have the ability of sharing the data processing task and the part of the de-packetizing task with the same data processor and therefore provides all needed flexibility in the de-packetizing task.

The described arrangements have been advanced merely by way of explanation any many modifications may be made thereto without departing from the spirit and scope of the invention which includes every novel feature and combination of novel features herein disclosed.

CLAIMS:-

1. Apparatus for depacketizing and aligning packetized input data, having:

an input memory for receiving storing, and output of the input data, and for outputting of units of a payload of a data packet of the input data;

data processing means for receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating a payload size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal whereby to cause the payload units to be outputted from the input memory to the word formatter; and

an input buffer for receiving said data words from the word formatter and storing these, and for transferring the data words to the data processing means, to effect said separate receiving of said payload;

said data processing means for effecting said data processing using the received said data words.

2. Apparatus as claimed in claim 1 having a data input interface through which the input data is transferred to the input memory, said data input interface for performing hand shaking with a packetized data source of said input data.

3. Apparatus as claimed in claim 1 or claim 2 wherein the input memory has a fullness level detector for generating a level filled signal when the input data received thereby is such as to fill the input memory to a predetermined level, and said data processing means is responsive to generation of said level filled signal to execute said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating said payload size signal.

4. Apparatus as claimed in claim 3 having an interrupt controller, for receiving said level filled signal and generating an interrupt signal pursuant to receipt thereof, said data processing means being arranged for receipt of said interrupt signal and, on receipt thereof, for executing said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal.

5. Apparatus as claimed in claim 3 or claim 4, as appended directly or indirectly to claim 2, wherein the input memory has a further fullness level detector for generating and directing to said data input interface a further level filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, said data input interface being responsive to receipt of said further level filled signal to generate a data request signal for direction to said packetized data source, indicative of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source.

6. Apparatus as claimed in any preceding claim wherein the input memory is controlled whereby said input data comprising said packet is removed from the input memory and relaced by fresh input data, pursuant to the transfer to the data processing means of said words representing the data packet to the data the apparatus being arranged for repetitive depacketizing and aligning of data packets and data processing thereof, the data processing means being arranged for repetitively and alternatingly executing a step comprising said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal, and a step comprising said separately receiving and effecting data processing of the payload of the data packet.

7. Apparatus as claimed in any preceding claim wherein the data processing means includes a digital signal processor, data/program memory, DMA controller and input buffer, each in data communication via a bus.

8. Apparatus as claimed in claim 7, wherein the word formatter is arranged for generating a DMA request signal when a said data word is formed thereby, and the DMA controller is responsive to said DMA request signal to generate and direct a transfer signal to the digital signal

processor, the digital signal processor being responsive to the transfer signal to enable the DMA controller to move the data word from the word formatter to the input buffer for subsequent processing.

9. Apparatus as claimed in claim 5 wherein said input memory is a first in first out memory.

10. Apparatus as claimed in any preceding claim wherein the data processing means is arranged to execute said detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID.

11. Apparatus as claimed in any preceding claim wherein the data processing means, pursuant to said detecting and identifying the data packet, extracts timing information from the input data.

12. Apparatus as claimed in any preceding claim wherein the data processing means, pursuant to said detecting and identifying the data packet, extracts side information from the input data.

13. A method for depacketizing and aligning packetized input data comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying and determining the size of a payload of a data packet of the input data outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal whereby to cause payload units which form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing these in said input buffer;

transferring said data words to the data processing means; and

effecting data processing on the data packet represented by the data words transferred thereto, using the transferred data words.

14. A method as claimed in claim 13 wherein the input data is transferred to the input memory via an data input interface which performs hand shaking with a packetized data source of said input data.

15. A method as claimed in claim 13 or claim 14 including the step of generating a level filled signal when the input data received by the input memory is such as to fill the input memory to a predetermined level, and causing said data processing means to effect said detecting, identifying and determining payload size of the data packet, and to said generate payload size signal, pursuant to generation of the level filled signal.

16. A method as claimed in claim 3 including the step of generating an interrupt signal from said level filled signal and directing said interrupt signal to said data processing means to cause said data processing means to effect said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and to generate said payload size signal.

17. A method as claimed in claim 15 or claim 16, as appended directly or indirectly to claim 14, including the step of generating and directing to said data input interface a further level filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, and causing said data input interface to generate, responsive to receipt thereby of said further level filled signal, a data request signal for direction to said packetized data source, indicative of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source,

18. A method as claimed in any one of claims 13 to 17 wherein the input memory is controlled whereby said input data comprising a said packet is removed from the input memory and relaced by fresh input data pursuant to the transfer of said words representing that data packet to the data processor, and wherein a step comprising said receiving the outputted input

data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal indicative of the size of the payload, and a step comprising effecting data processing of the payload are repetitively and alternatingly executed.

19. A method as claimed in claim 18, including generating a DMA request signal when a said word is formed, and applying the DMA request signal to a digital signal processor forming part of said data processing means to cause the digital signal processor to enable a DMA controller to move that data word from the word formatter to an input buffer of the data processor for subsequent processing.

20. A method as claimed in any one of claims 13 to 19 wherein said input memory is a first in first out memory.

21. A method as claimed in any one of claims 13 to 20 wherein the data processing means executes said detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID.

22. A method as claimed in any one of claims 13 to 21 wherein the data processing means extracts timing information from the input data pursuant to said detecting and identifying the data packet.

23. A method as claimed in any one of claims 13 to 22 wherein the data processing means extracts side information from the input data pursuant to said detecting and identifying the data packet.

24. Apparatus for depacketizing and aligning packetized input data, having:

an input memory for receiving storing, and output of the input data, and for outputting of units of a payload of a data packet of the input data;

data processing means for receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating a payload

size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal whereby to cause the payload units to be outputted from the input memory to the word formatter; and

means for transferring the data words to the data processing means, to effect said separate receiving of said payload.

25. A method for depacketizing and aligning packetized input data comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying and determining the size of a payload of a data packet of the input data outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal whereby to cause payload units which form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing these in said input buffer;

transferring said data words to the data processing means.

26. Apparatus for depacketising and aligning packetised input data, including data processing means which in use detects a payload of a data packet in the input data and processes the payload.

27. Apparatus as claimed in claim 26 wherein the data processing means repetitively and

alternatingly executes functions of detecting payloads and processing these.

28. A method for depacketizing and aligning packetized input data wherein functions of detecting a payload of a data packet in the input data and processing the payload are effected separately by the same data processing means.

29. A method as claimed in claim 28, wherein said functions are repetitvely and alternatingly executed with respect to successive data packets in the input data.

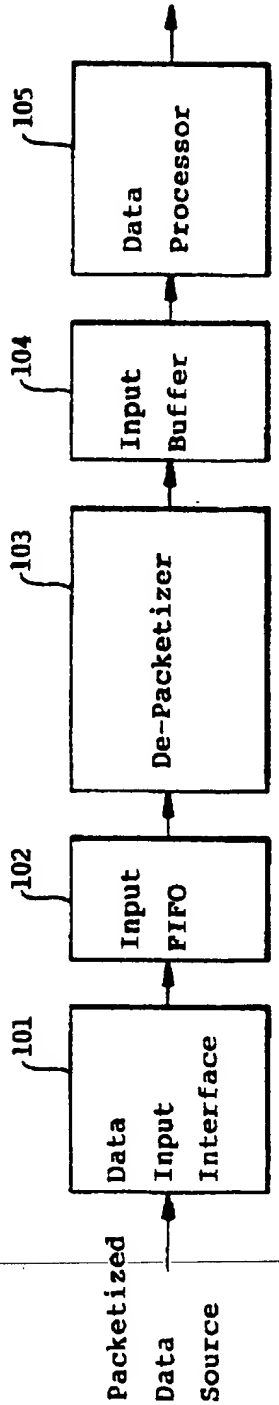

FIGURE 1 (Prior Art)

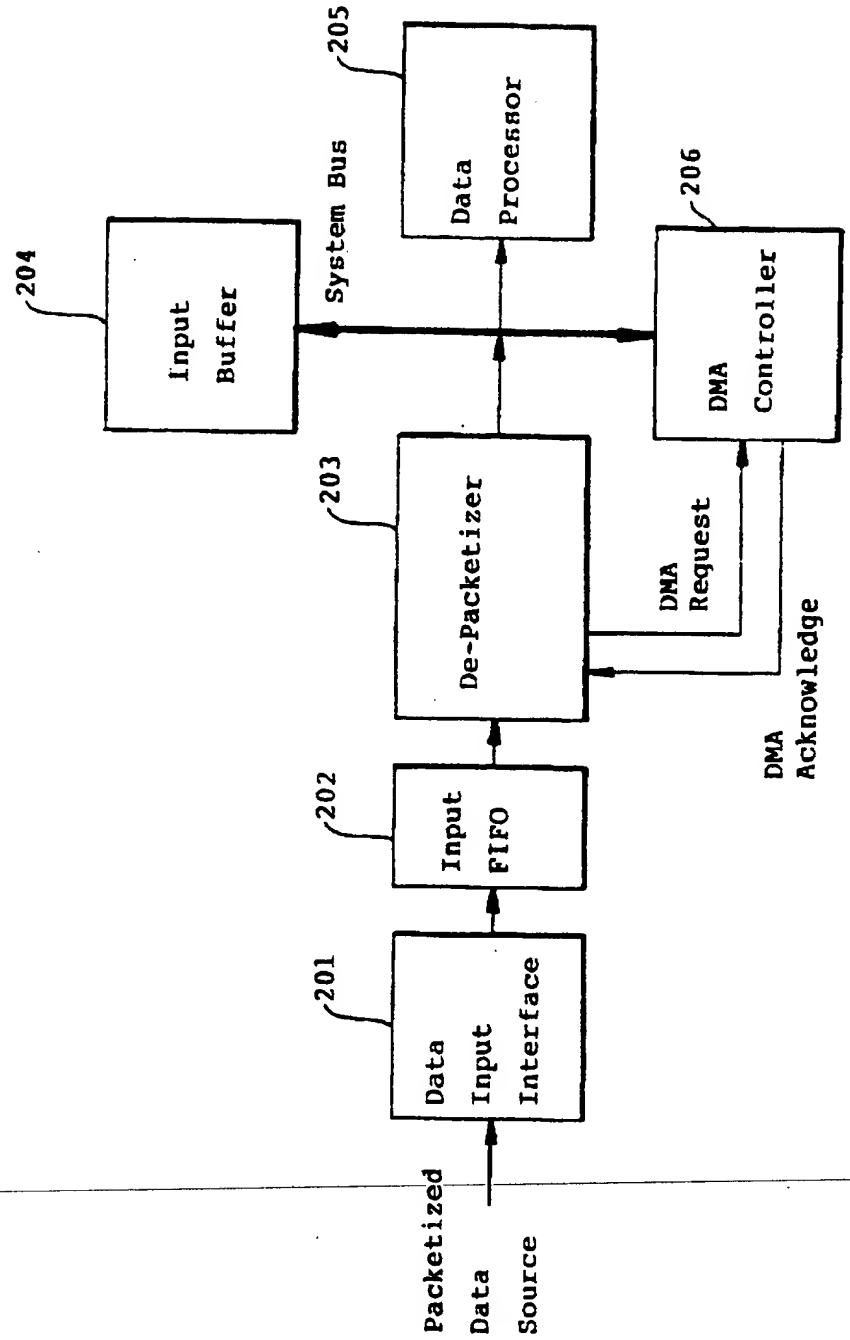

FIGURE 2 (Prior Art)

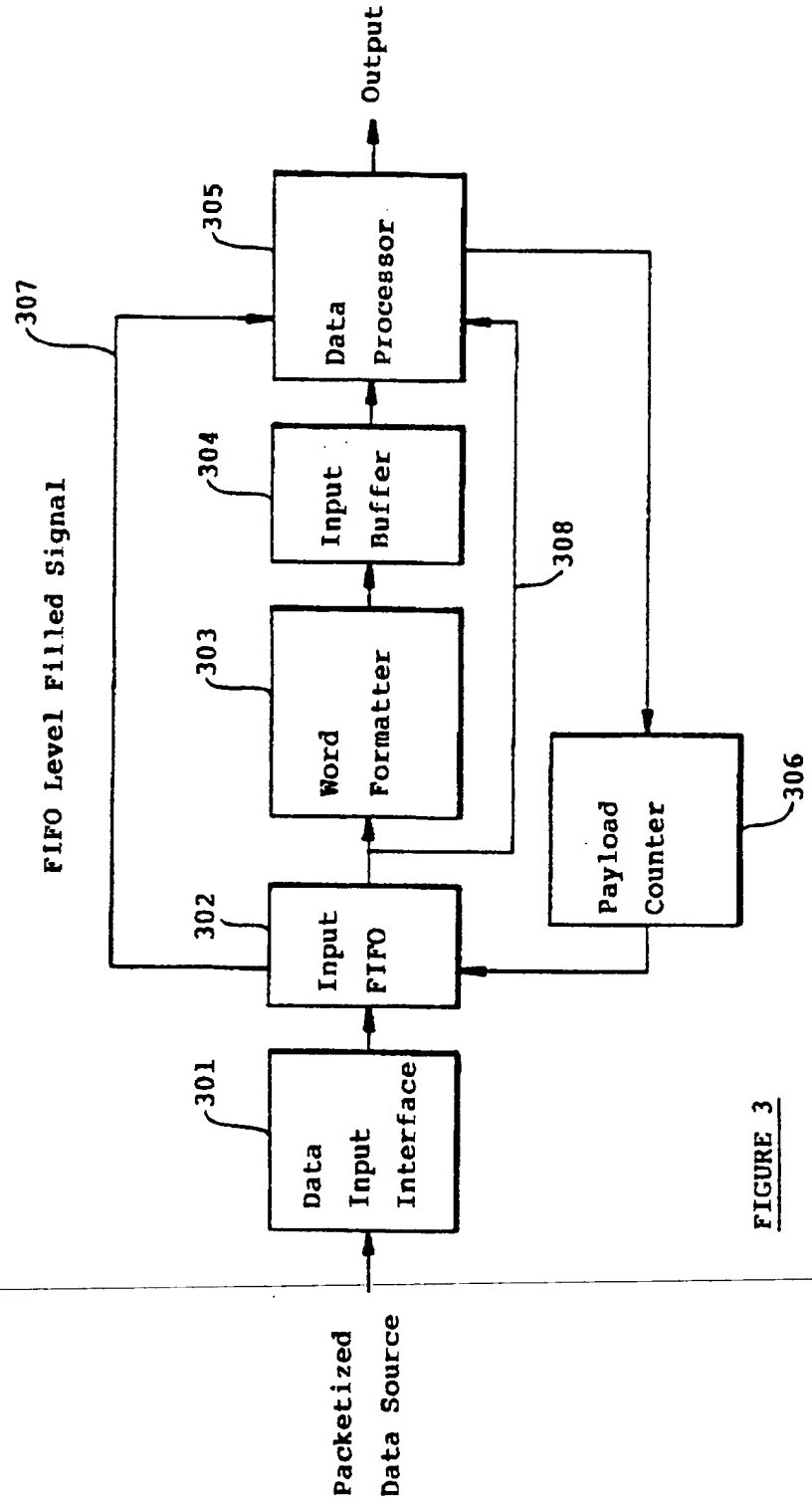
Packetized Data Source
Data Input Interface
301
Input FIFO
302
Word Formatter
303
Input Buffer
304
Data Processor
305
Output
Payload Counter
306
FIFO Level Filled Signal
307
308

FIGURE 3

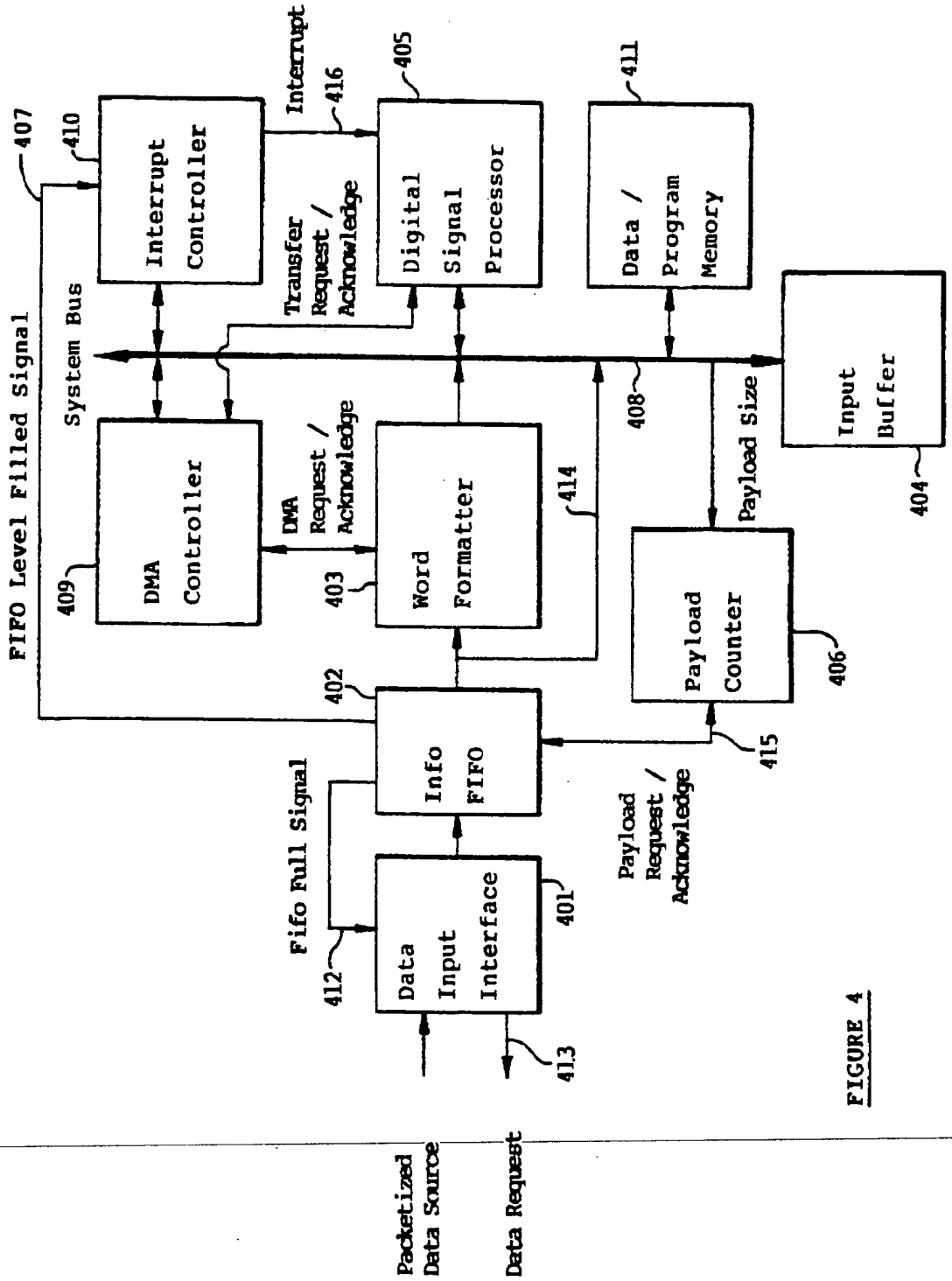
Interrupt Controller
410
Interrupt
416
Digital Signal Processor
405
Data / Program Memory
411
407
FIFO Level Filled Signal
System Bus
Transfer Request / Acknowledge
DMA Controller
409
DMA Request / Acknowledge
Word Formatter
403
414
408
Payload Size
Input Buffer
404
Payload Counter
406
402
Info FIFO
415
Payload Request / Acknowledge
Fifo Full Signal
412
Data Input Interface
401
413
Packetized Data Source
Data Request

FIGURE 4

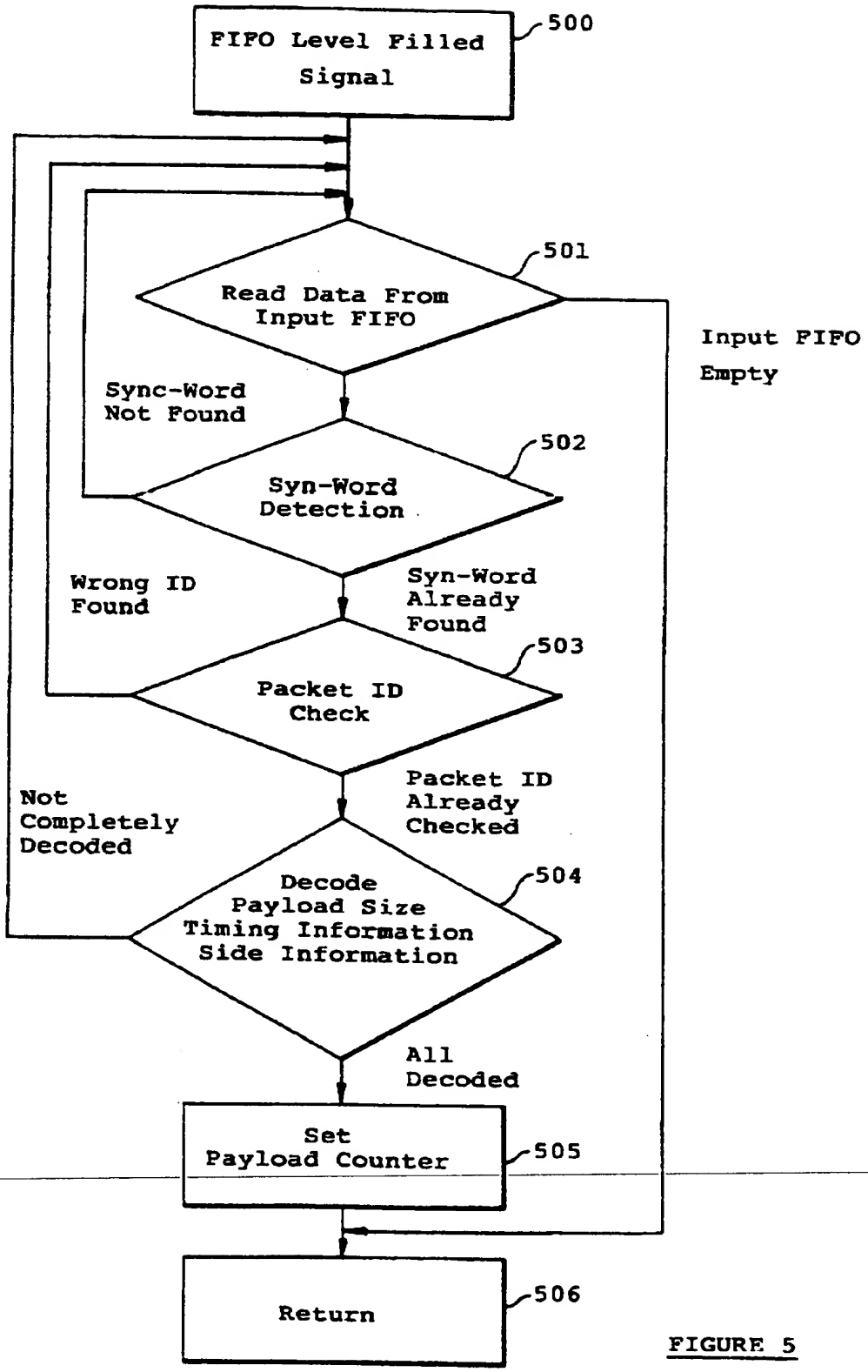
FIFO Level Filled Signal
500
Read Data From Input FIFO
501
Input FIFO Empty
Sync-Word Not Found
Syn-Word Detection
502
Wrong ID Found
Syn-Word Already Found
Packet ID Check
503
Not Completely Decoded
Packet ID Already Checked
Decode Payload Size Timing Information Side Information
504
All Decoded
Set Payload Counter
505
Return
506

FIGURE 5

INTERNATIONAL SEARCH REPORT

[redacted] Application No
PCT/SG 97/00055

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04J3/06

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DOBINSON R W ET AL: "INTERFACING TO ETHERNET USING VLSI PROTOCOL CHIPS" INTERFACES IN COMPUTING, vol. 3, no. 3/04, September 1985, pages 173-187, XP002005672 see page 174, line 10 - line 24 see page 178, line 5 - line 41 see page 179, line 6 - line 139 ---	26,28
A	DE 42 17 911 A (BUNDESREP DEUTSCHLAND) 2 December 1993 see column 1, line 64 - column 2, line 62 ---	1,13,24, 25
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 July 1998	24/07/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Van den Berg, J.G.J.

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INTERNATIONAL SEARCH REPORT

Ir. a[redacted]pplication No
PCT/SG 97/00055

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 798 932 A (MATSUSHITA ELECTRIC IND CO LTD) 1 October 1997 see page 5, line 20 - line 25 see page 6, line 35 - line 41 see page 7, line 21 - line 27 see page 8, line 22 - line 46 see page 11, line 55 - page 12, line 8	1,13,24, 25
A	US 5 534 937 A (ZHU QIN-FAN ET AL) 9 July 1996 see column 3, line 3 - line 13 see column 3, line 59 - column 4, line 16 see column 4, line 58 - line 62	1,13,24, 25
A	EP 0 648 034 A (BELL TELEPHONE MFG ;ALCATEL NV (NL)) 12 April 1995 see column 2, line 32 - line 45 see column 3, line 54 - column 4, line 18 see column 8, line 33 - line 42 see column 9, line 12 - line 24	2

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Ir. application No
PCT/SG 97/00055

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 4217911 A	02-12-1993	NONE	
EP 0798932 A	01-10-1997	JP 10093960 A	10-04-1998
US 5534937 A	09-07-1996	EP 0704134 A	03-04-1996
		JP 8511932 T	10-12-1996
		WO 9528802 A	26-10-1995
EP 0648034 A	12-04-1995	US 5453980 A	26-09-1995